<u>In the Drawings</u>

Figure 1: Add label "EXTERNAL PERIPHERALS" to element 82.

Figure 7A (second occurrence) Change to "FIG. 7B."
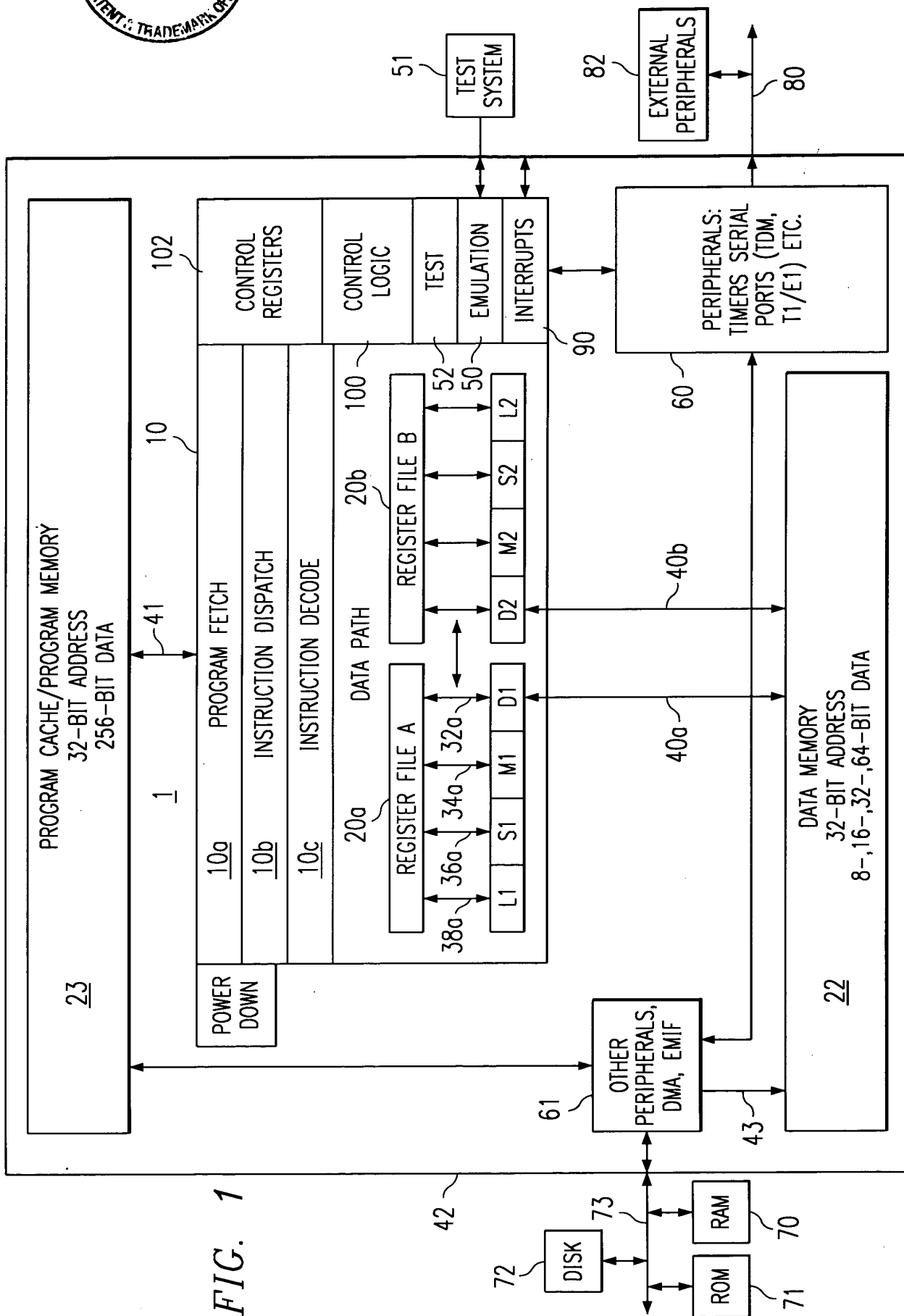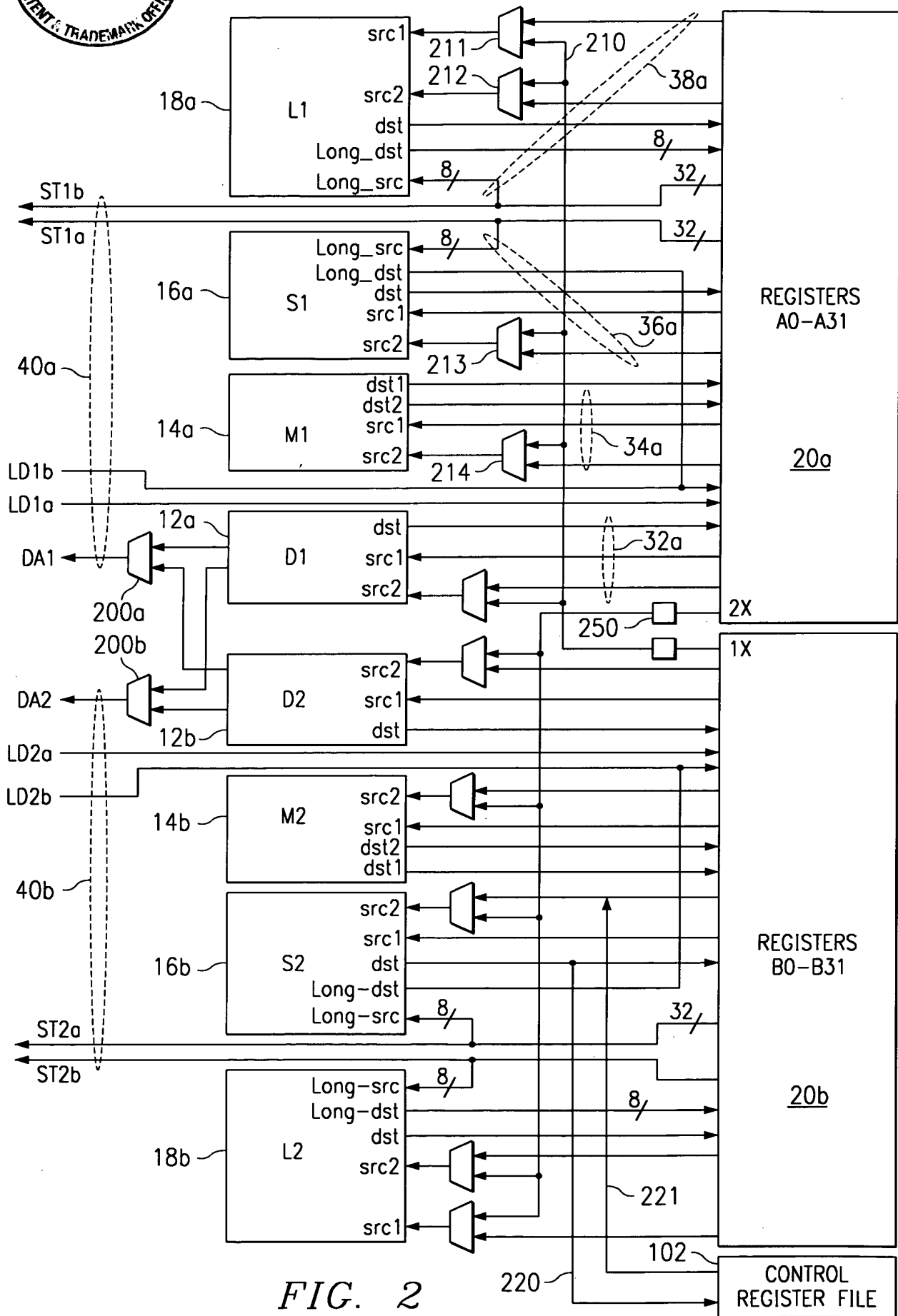
FIG. 1

FIG. 2

FIG. 3

LSBs OF THE BYTE ADDRESS

31 0	31 0	31 0	31 0	31 0	31 0	31 0	31 0
IP	IP	IP	IP	IP	IP	IP	IP

INSTRUCTION A 000002, INSTRUCTION B 001002, INSTRUCTION C 010002, INSTRUCTION D 011002, INSTRUCTION E 100002, INSTRUCTION F 101002, INSTRUCTION G 110002, INSTRUCTION H 111002

FIG. 4A

31 0	31 0	31 0	31 0	31 0	31 0	31 0	31 0
10	10	10	10	10	10	10	10

INSTRUCTION A, INSTRUCTION B, INSTRUCTION C, INSTRUCTION D, INSTRUCTION E, INSTRUCTION F, INSTRUCTION G, INSTRUCTION H

FIG. 4B

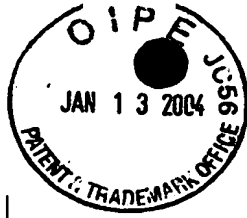| 31 0	31 0	31 0	31 0	31 0	31 0	31 0	31 0
11	11	11	11	11	11	11	11

INSTRUCTION A, INSTRUCTION B, INSTRUCTION C, INSTRUCTION D, INSTRUCTION E, INSTRUCTION F, INSTRUCTION G, INSTRUCTION H

FIG. 4C

31 0	31 0	31 0	31 0	31 0	31 0	31 0	31 0
10	10	11	11	10	11	11	10

INSTRUCTION A, INSTRUCTION B, INSTRUCTION C, INSTRUCTION D, INSTRUCTION E, INSTRUCTION F, INSTRUCTION G, INSTRUCTION H

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FIG. 5

CLOCK CYCLE

FETCH PACKET	EXECUTE PACKET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
n	k	PG	PS	PW	PR	DP	DC	E1	E2	E3	E4	E5												
n	k+1						DP	DC	E1	E2	E3	E4	E5											
n	k+2							DP	DC	E1	E2	E3	E4	E5										
n+1	k+3				PG	PS	PW	PR	DP	DC	E1	E2	E3	E4	E5									
n+2	k+4					PG	PS	PW	PR	DP	DC	E1	E2	E3	E4	E5								
n+3	k+5						PG	PS	PW	PR	DP	DC	E1	E2	E3	E4	E5							
n+4	k+6							PG	PS	PW	PR	DP	DC	E1	E2	E3	E4	E5						
n+5	k+7								PG	PS	PW	PR	DP	DC	E1	E2	E3	E4	E5					
n+6	k+8									PG	PS	PW	PR	DP	DC	E1	E2	E3	E4	E5				

FIG. 7A
(PRIOR ART)

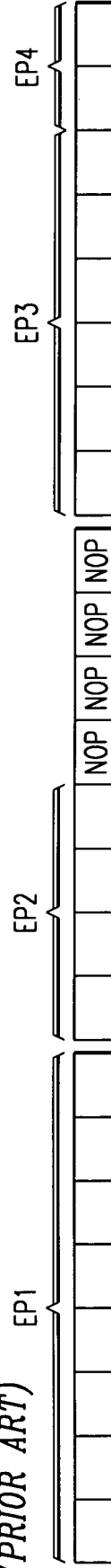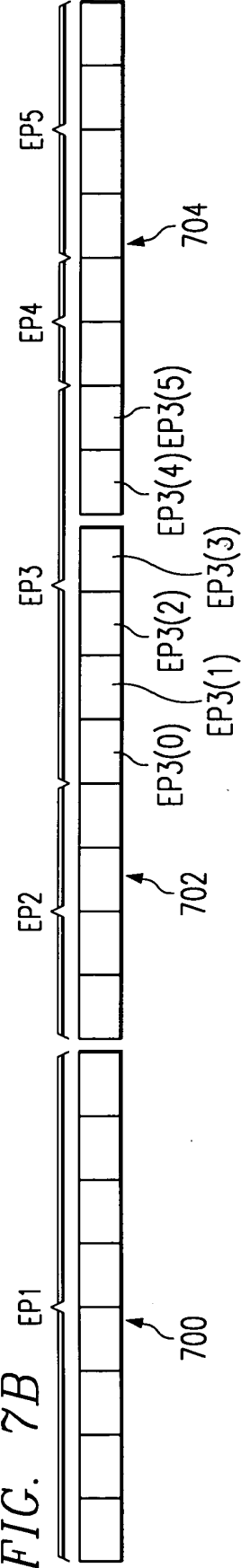EP1 700 EP2 EP3 [NOP NOP NOP NOP] EP4

FIG. 7B

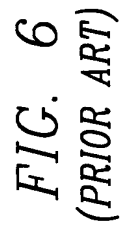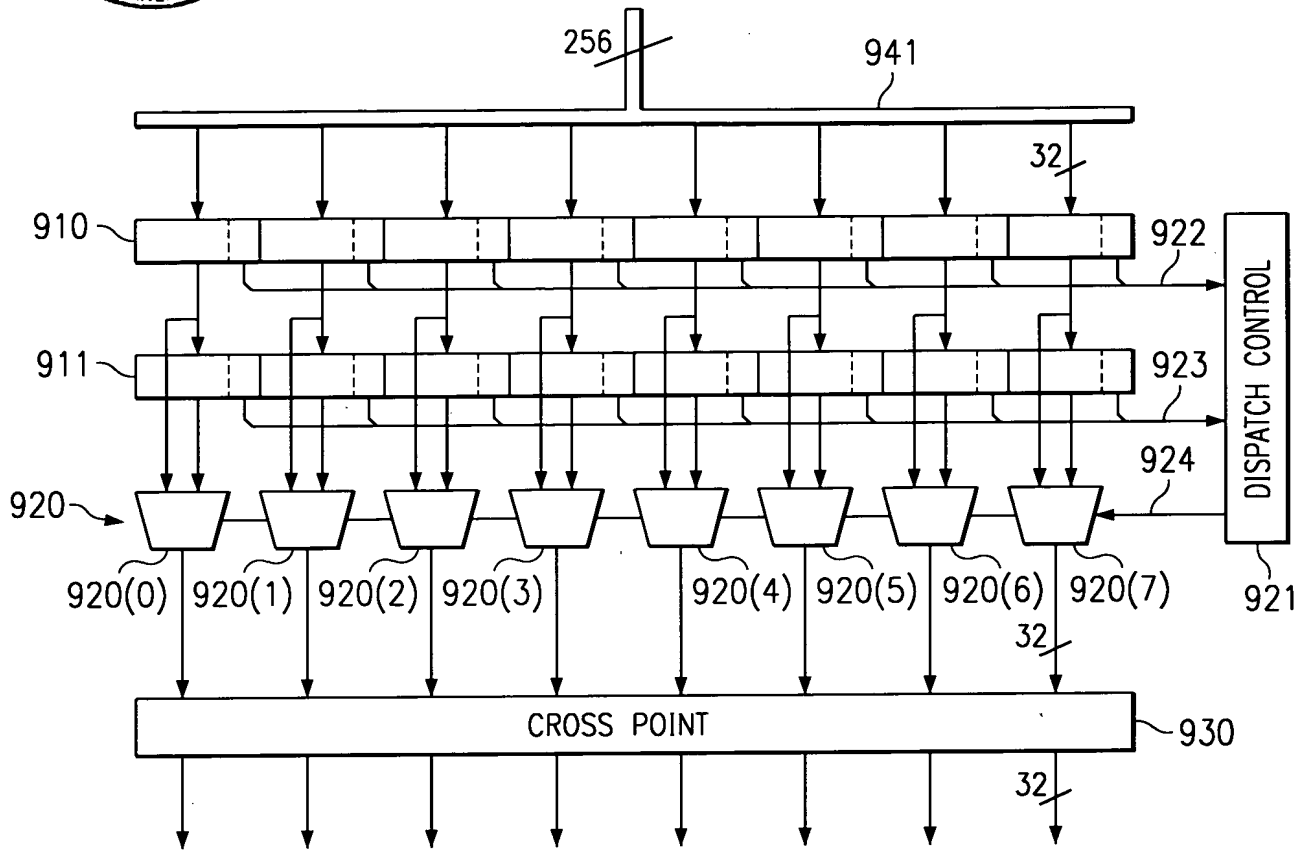EP1 700 EP2 702 EP3 [EP3(0) EP3(1) EP3(2) EP3(3) EP3(4) EP3(5)] EP4 704 EP5

FIG. 6
(PRIOR ART)

FIG. 8

FIG. 9

FIG. 11

FIG. 10